REMARKS:

This is in response to the Office Action dated August 1, 2001, which was paper #4 of the present application. Applicant amends claims 1, 3, 7, and 9 of the present application; marked up versions of the amended claims are attached hereto pursuant to 37 C.F.R. § 1.121(c)(ii). Pursuant to this amendment, claims 1-12 are pending in the application. Reexamination and reconsideration of the application are respectfully requested.

The Examiner objects to the title of the invention as not precise or non-descriptive. Applicant amends the title of the invention to address the Examiner's objection.

The Examiner rejects claims 1-3, 6-9, and 12 as anticipated by U.S. Patent No. 5,436,875 to Shinada *et al.* The Examiner also rejects claims 4-5 and 10-11 as obvious over the Shinada patent as applied to claims 1-3, 6-9, and 12. All of the Examiner's rejections are hereby respectfully traversed. Applicant, however, amends claims 1, 3, 7, and 9 only to better define aspects of the present application. For reasons stated below, applicant submits that all pending claims are in condition for allowance.

A conventional data recording device, such as a CD-R drive or a CD-RW drive, records data onto an optical disk. Oftentimes, the data recording device may have a high speed writing capability and can record data onto the disk at a speed faster than the speed it receives data from an external source. As a result, data writing by such data recording device is often performed intermittently, causing a waste of power problem.

The present application describes a recording data process device with a data processing circuit for recording data onto a disk, a control circuit controlling the data processing circuit for writing and/or reading data to and from the disk, and a buffer memory for temporarily storing the data to be recorded onto the disk or reproduced from the disk. In one aspect of the present invention, the control circuit controls data reading from or recording onto the disk based on the amount of data having been stored in the buffer memory. The control circuit suspends operation of

the data processing circuit by either interrupting the power supply or by halting the supply of an operation clock supplied to the data processing circuit until the data stored in the buffer memory reaches a predetermined amount. As a result, the presently described recording data process device reduces its power consumption when recording and/or reproducing data onto/from the disk. See Application, page 6, line 24-page 8, line 4, and page 16, lines 16-21. In another aspect, in resuming the recordation of data on the disk, the presently described recording device synchronizes the new data about to be recorded onto the disk and the data previously recorded on the disk immediately before the discontinuation of data recording. Therefore, the new recording data can be recorded in a region on the disk successive, and without break, to a region where the last recording data were recorded immediately before the discontinuation of data recording. See Application, page 11, line 23-page 12, line 5.

The Shinada patent describes a recording and/or reproducing apparatus for recording and/or reproducing data onto or from an optical disk. According to the Shinada patent, the recording/reproducing apparatus includes an encoder for outputting the audio data at the data transmission speed of 0.3 Mbit/s to the memory, which in turn outputs the audio data at the data transmission speed of 1.4 Mbit/s. Namely, when recording data onto the disk, the memory described in the Shinada patent outputs its audio data stored therein at a faster transmission speed than the audio data being fed into the memory by the encoder. Accordingly, the Shinada's recording/reproducing apparatus stops its recording function temporarily if the audio data stored in the memory becomes ***below*** a prescribed value. See FIG. 1, col. 6, lines 6-23 of the Shinada patent. This aspect of the Shinada patent differs from the presently described recording device which suspends the operation of the data processing circuit ***until*** the data stored in the buffer memory reaches a predetermined value. In addition, the Shinada patent stops its recording function for better data continuity. That patent does not describe suspending a data processing circuit by interrupting the power supply nor by withholding the

operation clock supplied to the data processing circuit, thereby reducing its power consumption during operation.

Furthermore, the Shinada patent does not describe synchronizing the new data to be recorded onto the disk with the last recorded data immediately before the discontinuation of data recording, thereby assuring the new data would be recorded in a region successive without break to the region where the last recording data is recorded. Therefore, aspects of the present invention distinguish over the Shinada patent.

Claim 1 of the present application recites, in pertinent part, "said data processing circuit for recording data being placed in a suspended state by interrupting the power supply or by halting the supply of an operation clock." As discussed, the Shinada patent does not describe this limitation of claim 1. Thus, claim 1 distinguishes over the Shinada patent and is in condition for allowance.

Claim 2 depends on claim 1. Thus, claim 1 similarly distinguishes over the Shinada patent and is in condition for allowance.

Claim 3 depends on claim 1. Moreover, claim 3 further recites, in pertinent part, "said data processing circuit being operated in synchronism with a reproduction clock obtained by reproducing the data already recorded on the disk." As discussed, the Shinada patent neither describes the above-mentioned limitation of claim 1 nor this limitation of claim 3. Thus, claim 3 distinguishes over the Shinada patent and is in condition for allowance.

Claims 4-6 depend on claim 3. Thus, claims 4-6 similarly distinguish over the Shinada patent and are in condition for allowance.

Claim 7 recites, in pertinent part, "said data processing circuit being placed in a suspended state by interrupting the power supply or by halting the supply of an operation clock." As discussed, the Shinada patent does not describe this limitation of claim 7. Thus, claim 7 distinguishes over the Shinada patent and is in condition for allowance.

Claim 9 depends on claim 7. Moreover, claim 9 further recites, in pertinent part, "said data processing circuit being operated in synchronism with a

reproduction clock obtained by reproducing the data already recorded on the disk." As discussed, the Shinada patent neither describes the above-mentioned limitation of claim 7 nor this limitation of claim 9. Thus, claim 9 distinguishes over the Shinada patent and is in condition for allowance.

Claims 10-12 depend on claim 9. Thus, claims 10-12 similarly distinguish over the Shinada patent and are in condition for allowance.

The art made of record but not relied upon by the Examiner has been considered. However, it is submitted that this art neither describes nor suggests the presently claimed invention.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6700 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

HOGAN & HARTSON L.L.P.

Date: October 26, 2001

By: _____

Wei-Fu Hsu
Registration No. 45,723
Attorney for Applicant(s)

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Phone: 213-337-6700
Fax: 213-337-6701

Version with markings to show changes made:

1. (Amended) A recording data processing circuit for processing received data sent at a slower data transmission speed than a data processing speed at which to write recording data onto a disk, comprising:

a buffer memory for temporarily storing the received data;

a data processing circuit for preparing the recording data to record onto the disk, based on the received data read from the buffer memory; and

a system control circuit for controlling writing and reading of the received data with respect to the buffer memory, and operation of the data processing circuit,

wherein

the system control circuit suspends operation of the data processing circuit until an amount of received data equivalent to a predetermined writing capacity has been stored in the buffer memory, and releases suspension of the operation of the data processing circuit when an amount of received data equivalent to the predetermined writing capacity has been stored in the buffer memory, said data processing circuit for recording data being placed in a suspended state by interrupting the power supply or by halting the supply of an operation clock.

3. (Amended) A recording data processing device according to claim 2, wherein the system control circuit synchronizes the recording data to be newly recorded onto the disk, supplied from the data processing circuit to the writing circuit, with recording data recorded on the disk, said data processing circuit being operated in synchronism with a reproduction clock obtained by reproducing the data already recorded on the disk.

7. (Amended) A recording data processing circuit for processing received data sent at a slower data transmission speed than a data processing speed at which to write recording data onto a disk, and recording the recording data onto the disk, comprising:

a buffer memory for temporarily storing the received data;

a data processing circuit for preparing the recording data to record onto the disk, based on the received data read from the buffer memory;

a system control circuit for controlling writing and reading of the received data with respect to the buffer memory, and operation of the data processing circuit, and

a writing circuit for writing the recording data supplied from the data processing circuit onto the disk,

wherein

the system control circuit suspends operation of the data processing circuit and writing of the recording data onto the disk by the writing circuit until an amount of received data equivalent to a predetermined writing capacity has been stored in the buffer memory, and releases suspension of the operation of the data processing circuit to resume writing of the recording data onto the disk by the writing circuit when an amount of received data equivalent to the predetermined writing capacity has been stored in the buffer memory, said data processing circuit being placed in a suspended state by interrupting the power supply or by halting the supply of an operation clock.

9. (Amended) A recording data processing device according to claim 8, wherein the system control circuit synchronizes the recording data to be newly recorded onto the disk, supplied from the data processing circuit to the writing circuit, with recording data recorded on the disk, said data processing circuit being operated in synchronism with a reproduction clock obtained by reproducing the data already recorded on the disk.